Figure 1 Block Diagram of Preferred Multi Channel Desynchronizer

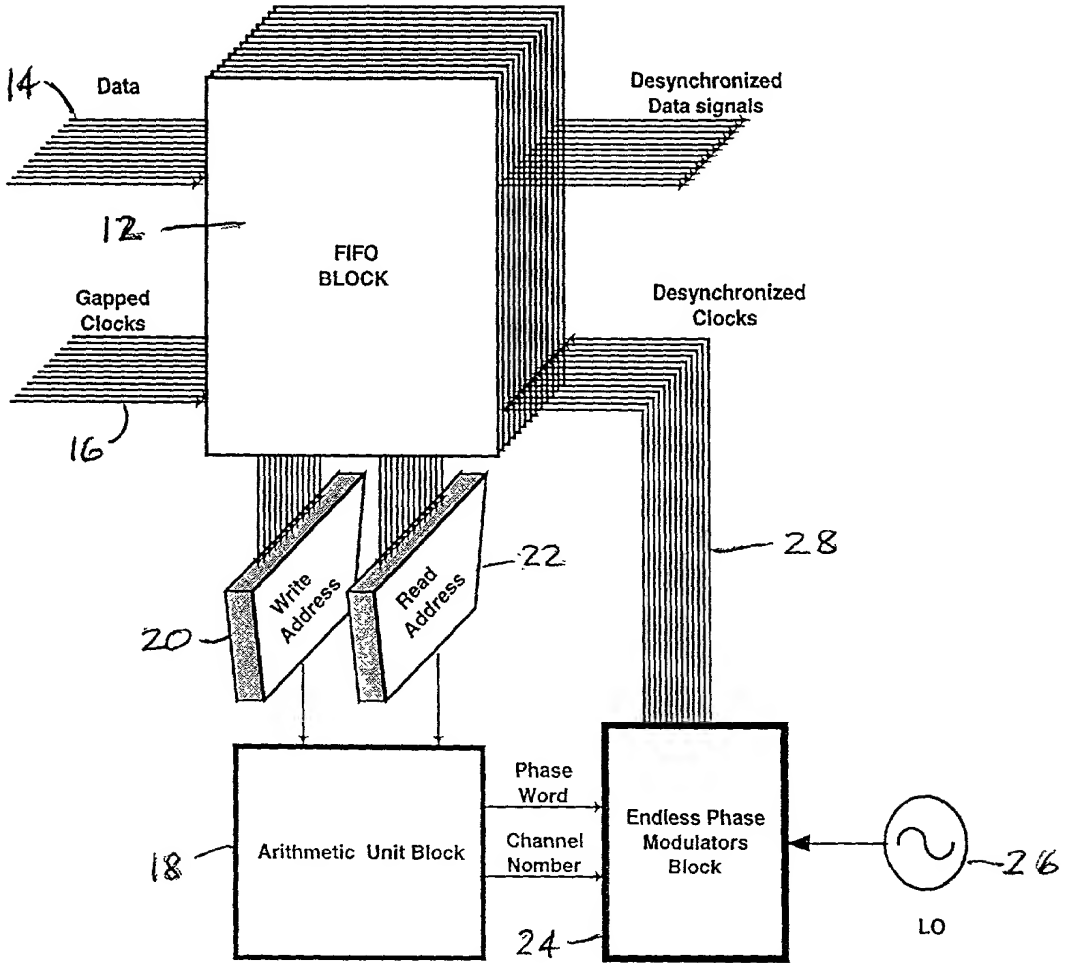

Fig. 1

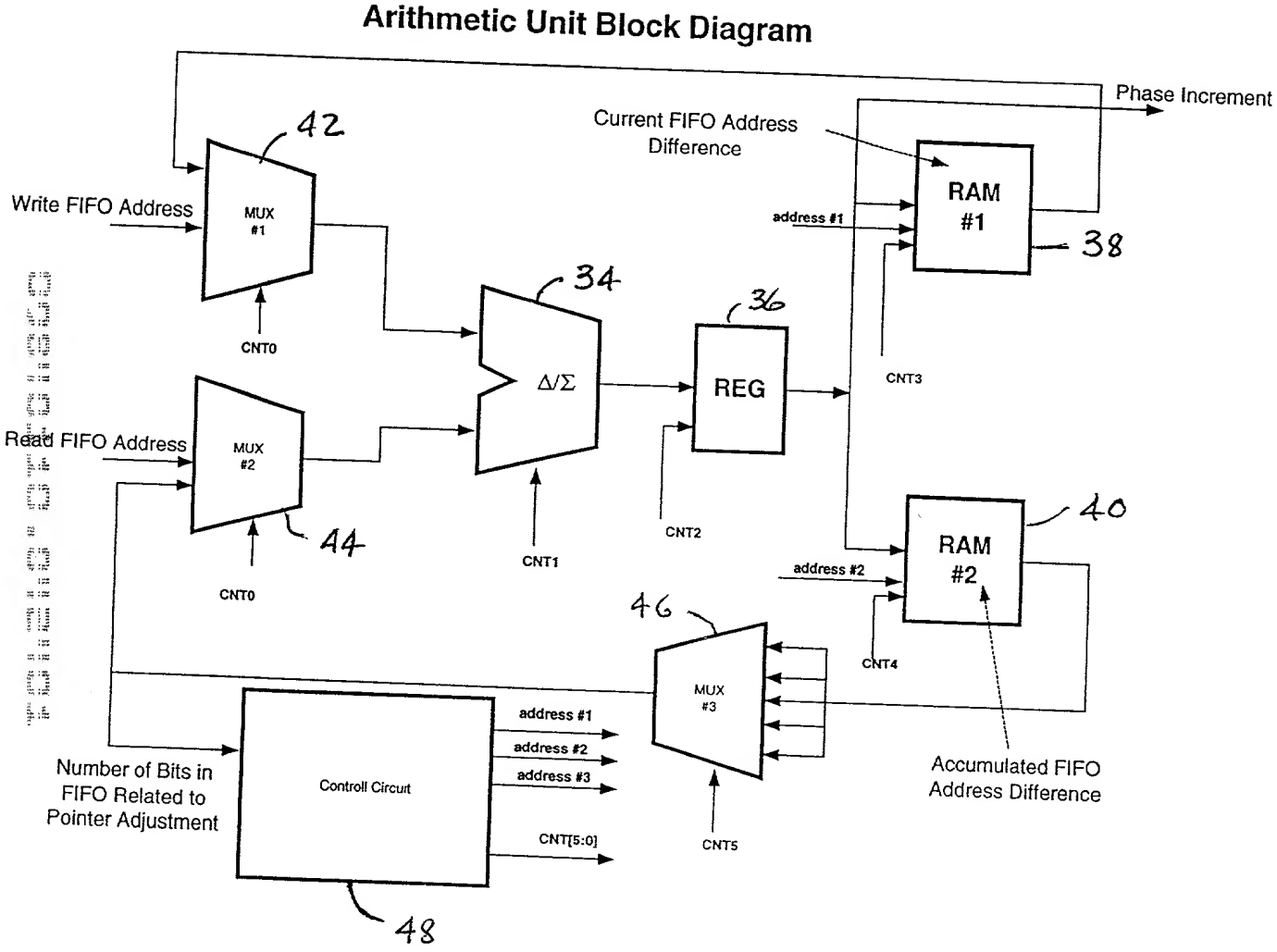
Arithmetic Unit Block Diagram
Phase Increment
Current FIFO Address Difference
42
Write FIFO Address
MUX #1
CNT0
34
Δ/Σ
36
REG
RAM #1
38
address #1
CNT3
Read FIFO Address
MUX #2
44
CNT0
CNT1
CNT2
40
RAM #2
address #2
CNT4
46
MUX #3
address #1
address #2
address #3
CNT[5:0]
CNT5
Number of Bits in FIFO Related to Pointer Adjustment
Controll Circuit
48
Accumulated FIFO Address Difference

Fig 2

Memory Map of RAM#1 for desynchronizing 12 channels of DS3 signal dropped from OC-12 signal

Ch#1 FIFO Address Difference
Ch#2 FIFO Address Difference
Ch#3 FIFO Address Difference
Ch#4 FIFO Address Difference
Ch#5 FIFO Address Difference
Ch#6 FIFO Address Difference
Ch#7 FIFO Address Difference
Ch#8 FIFO Address Difference
Ch#9 FIFO Address Difference
Ch#10 FIFO Address Difference
Ch#11 FIFO Address Difference
Ch#12 FIFO Address Difference
0
8
1/64 of UI Phase Increment
1/64

NOTE: N can be chosen for specific leak rate. Few more addresses can be added to the RAM#1 address space to enable adaptive bit leak rate!

Memory Map of RAM#2 for desynchronizing 12 channels of DS3 signal dropped from OC-12 signal

Ch#1 Accumulated FIFO Address Difference
Ch#2 Accumulated FIFO Address Difference
Ch#3 Accumulated FIFO Address Difference
Ch#4 Accumulated FIFO Address Difference
Ch#5 Accumulated FIFO Address Difference
Ch#6 Accumulated FIFO Address Difference
Ch#7 Accumulated FIFO Address Difference
Ch#8 Accumulated FIFO Address Difference
Ch#9 Accumulated FIFO Address Difference
Ch#10 Accumulated FIFO Address Difference
Ch#11 Accumulated FIFO Address Difference
Ch#12 Accumulated FIFO Address Difference
Ch#1 Pointer Adjustment Bits #
Ch#2 Pointer Adjustment Bits #
Ch#3 Pointer Adjustment Bits #
Ch#4 Pointer Adjustment Bits #
Ch#5 Pointer Adjustment Bits #
Ch#6 Pointer Adjustment Bits #
Ch#7 Pointer Adjustment Bits #
Ch#8 Pointer Adjustment Bits #
Ch#9 Pointer Adjustment Bits #
Ch#10 Pointer Adjustment Bits #
Ch#11 Pointer Adjustment Bits #
Ch#12 Pointer Adjustment Bits #
Spare Address for Holding Intermediate Values

Fig. 3

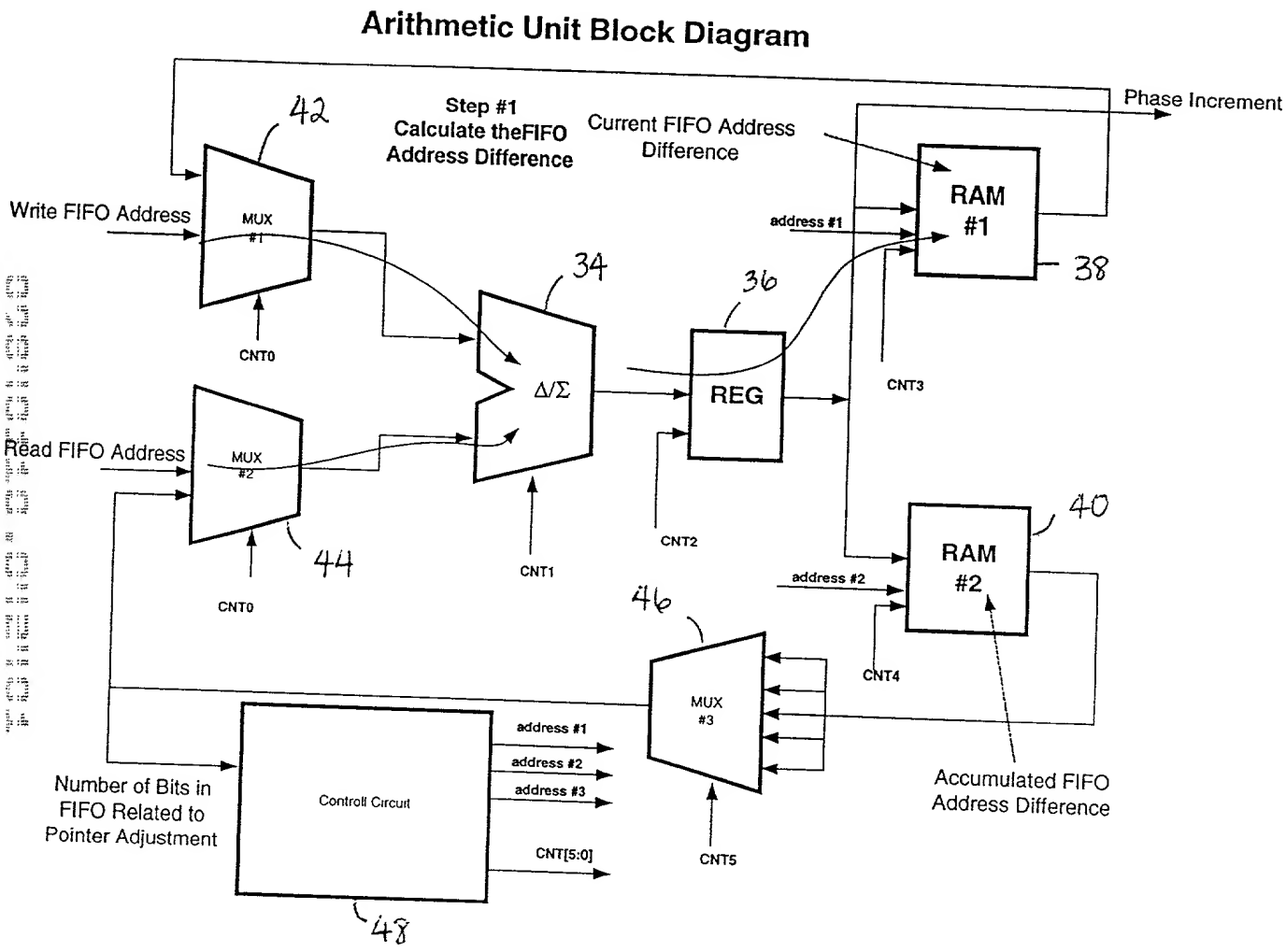
Arithmetic Unit Block Diagram
Step #1
Calculate theFIFO
Address Difference
Current FIFO Address
Difference
Phase Increment
42
Write FIFO Address
MUX
#1
CNT0
34
Δ/Σ
36
REG
RAM
#1
38
address #1
CNT3
Read FIFO Address
MUX
#2
CNT0
44
CNT1
CNT2
40
RAM
#2
address #2
CNT4
46
MUX
#3
CNT5
Number of Bits in
FIFO Related to
Pointer Adjustment
Controll Circuit
address #1
address #2
address #3
CNT[5:0]
48
Accumulated FIFO
Address Difference

Fig. 4

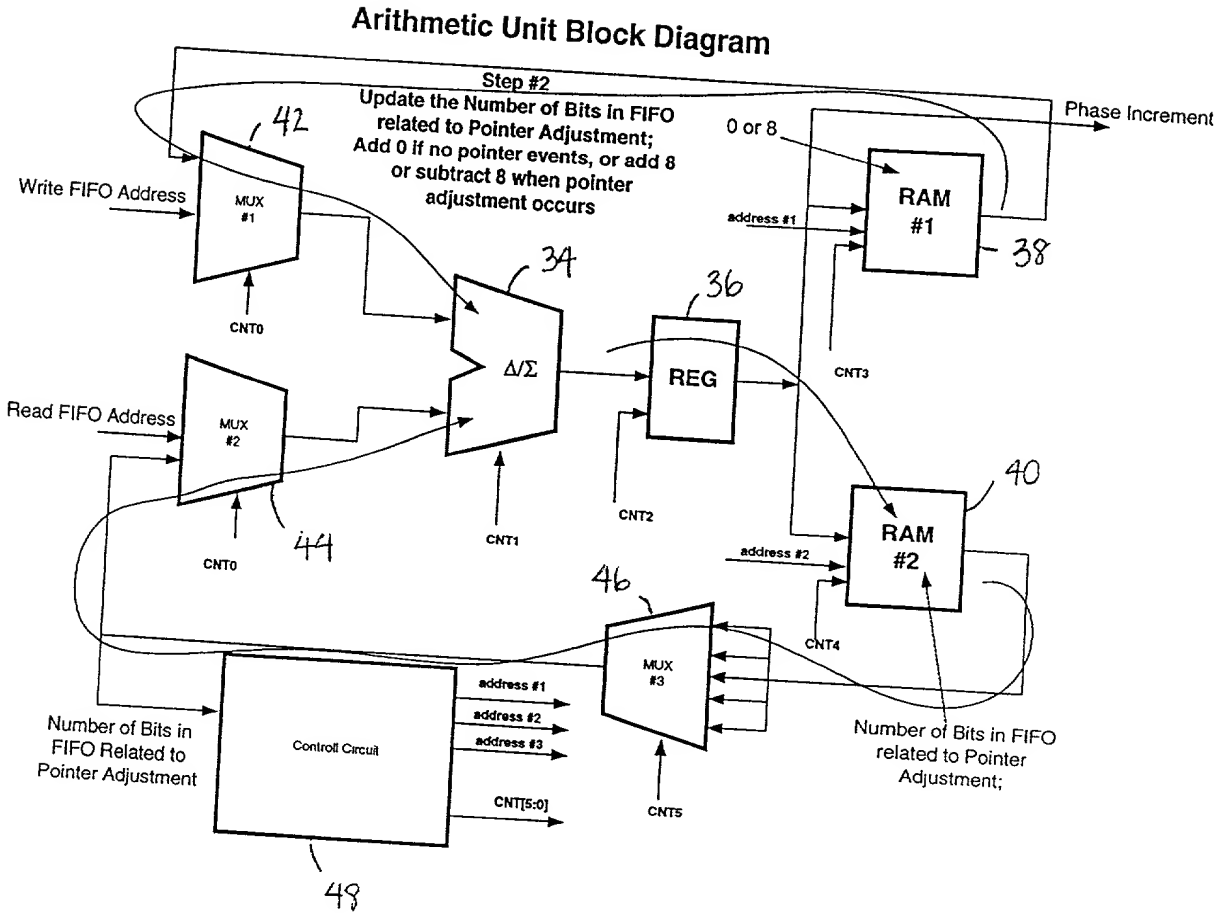
Arithmetic Unit Block Diagram
Step #2
Update the Number of Bits in FIFO related to Pointer Adjustment; Add 0 if no pointer events, or add 8 or subtract 8 when pointer adjustment occurs
Phase Increment
0 or 8
Write FIFO Address
MUX #1
42
CNT0
34
Δ/Σ
36
REG
RAM #1
38
address #1
CNT3
Read FIFO Address
MUX #2
CNT0
44
CNT1
CNT2
40
RAM #2
address #2
46
CNT4
MUX #3
address #1
address #2
address #3
CNT[5:0]
CNT5
Number of Bits in FIFO Related to Pointer Adjustment
Controll Circuit
48
Number of Bits in FIFO related to Pointer Adjustment;

Fig. 5

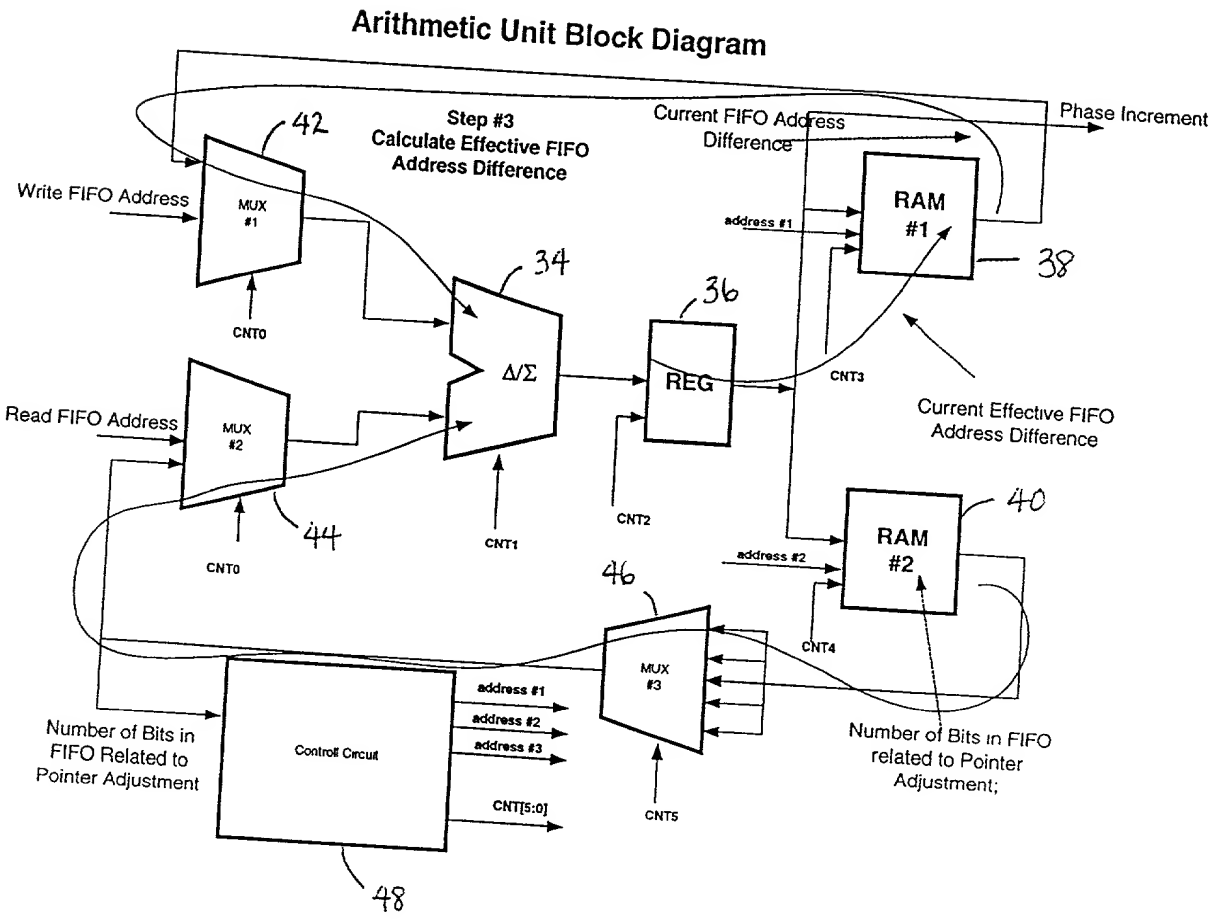
Arithmetic Unit Block Diagram
Step #3
Calculate Effective FIFO
Address Difference
Phase Increment
Current FIFO Address
Difference
42
Write FIFO Address
MUX
#1
CNT0
34
Δ/Σ
36
REG
RAM
#1
38
address #1
CNT3
Current Effective FIFO
Address Difference
Read FIFO Address
MUX
#2
CNT0
44
CNT1
CNT2
40
RAM
#2
address #2
46
CNT4
MUX
#3
CNT5
address #1
address #2
address #3
CNT[5:0]
Control Circuit
Number of Bits in
FIFO Related to
Pointer Adjustment
Number of Bits in FIFO
related to Pointer
Adjustment;
48

Fig. 6

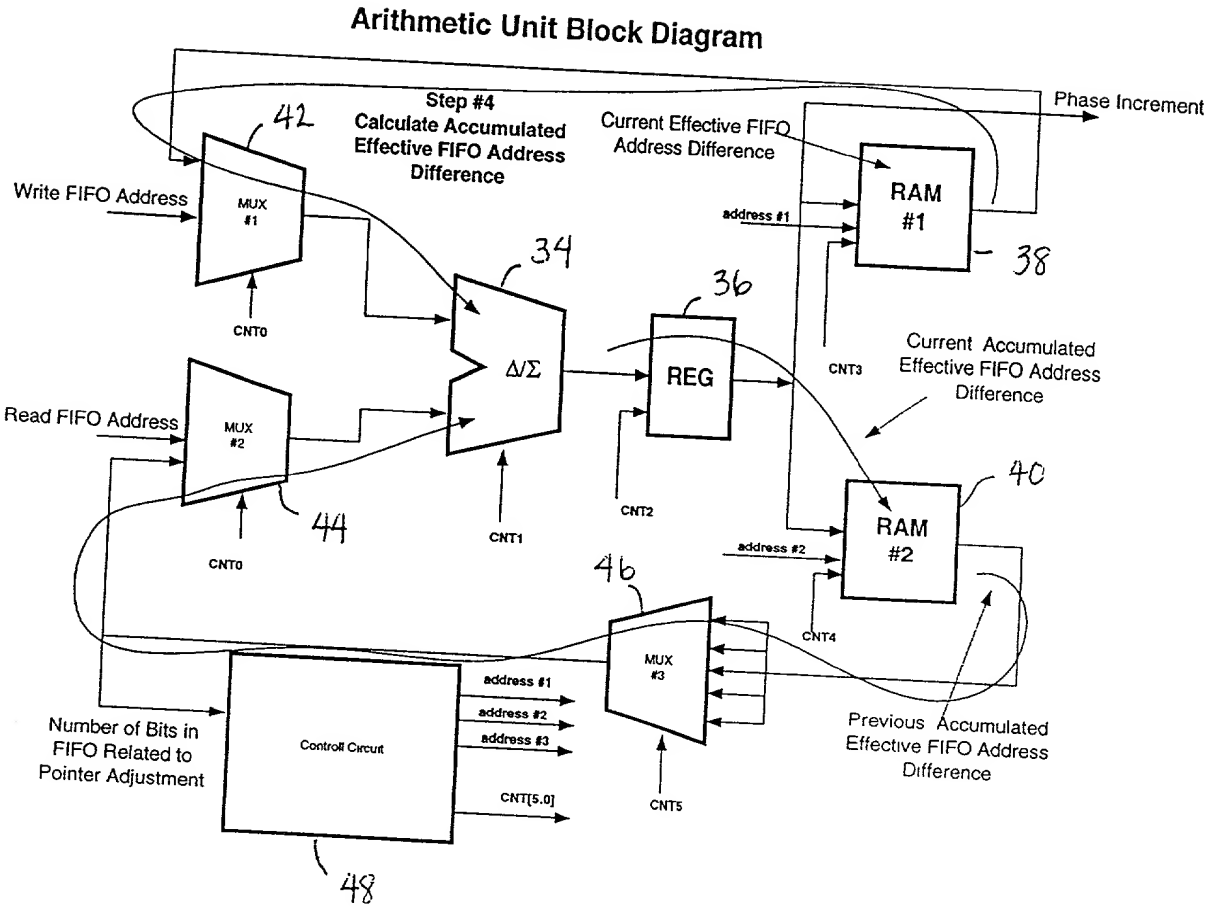
Arithmetic Unit Block Diagram
Step #4
Calculate Accumulated
Effective FIFO Address
Difference
Phase Increment
Current Effective FIFO
Address Difference
Write FIFO Address
MUX
#1
42
CNT0
34
Δ/Σ
36
REG
RAM
#1
38
address #1
CNT3
Current Accumulated
Effective FIFO Address
Difference
Read FIFO Address
MUX
#2
44
CNT0
CNT1
CNT2
40
RAM
#2
address #2
CNT4
46
MUX
#3
CNT5
address #1
address #2
address #3
CNT[5.0]
Controll Circuit
48
Number of Bits in
FIFO Related to
Pointer Adjustment
Previous Accumulated
Effective FIFO Address
Difference

Fig. 7

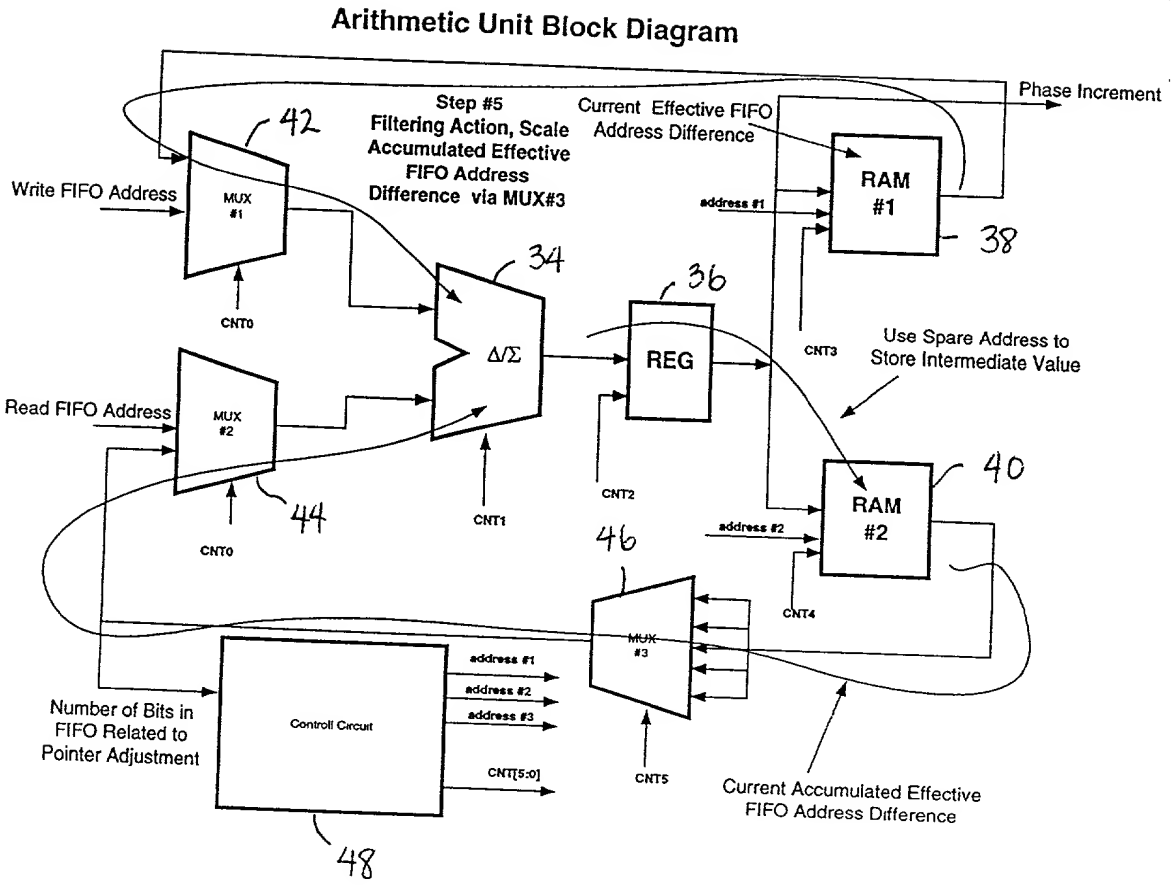
Arithmetic Unit Block Diagram
Step #5
Filtering Action, Scale
Accumulated Effective
FIFO Address
Difference via MUX#3
Current Effective FIFO
Address Difference
Phase Increment
42
Write FIFO Address
MUX
#1
CNT0
34
Δ/Σ
36
REG
RAM
#1
38
address #1
CNT3
Use Spare Address to
Store Intermediate Value
Read FIFO Address
MUX
#2
CNT0
44
CNT1
CNT2
40
RAM
#2
address #2
CNT4
46
MUX
#3
CNT5
address #1
address #2
address #3
CNT[5:0]
Controll Circuit
Number of Bits in
FIFO Related to
Pointer Adjustment
48
Current Accumulated Effective
FIFO Address Difference

Fig. 8

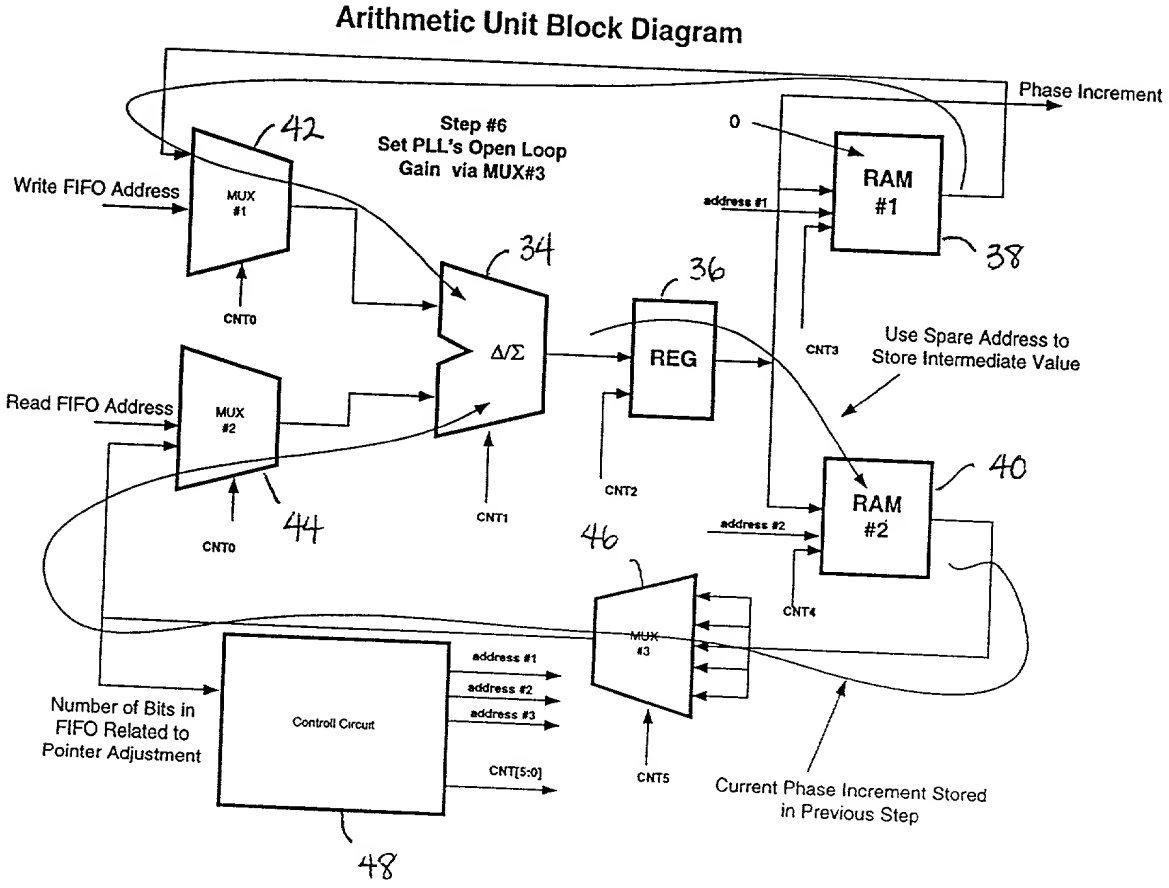
Arithmetic Unit Block Diagram
Phase Increment
Step #6
Set PLL's Open Loop
Gain via MUX#3
42
Write FIFO Address
MUX
#1
CNT0
34
Δ/Σ
36
REG
0
RAM
#1
address #1
38
CNT3
Use Spare Address to
Store Intermediate Value
Read FIFO Address
MUX
#2
CNT0
44
CNT1
CNT2
40
RAM
#2
address #2
CNT4
46
MUX
#3
address #1
address #2
address #3
CNT[5:0]
Controll Circuit
Number of Bits in
FIFO Related to
Pointer Adjustment
CNT5
Current Phase Increment Stored
in Previous Step
48

Fig. 9

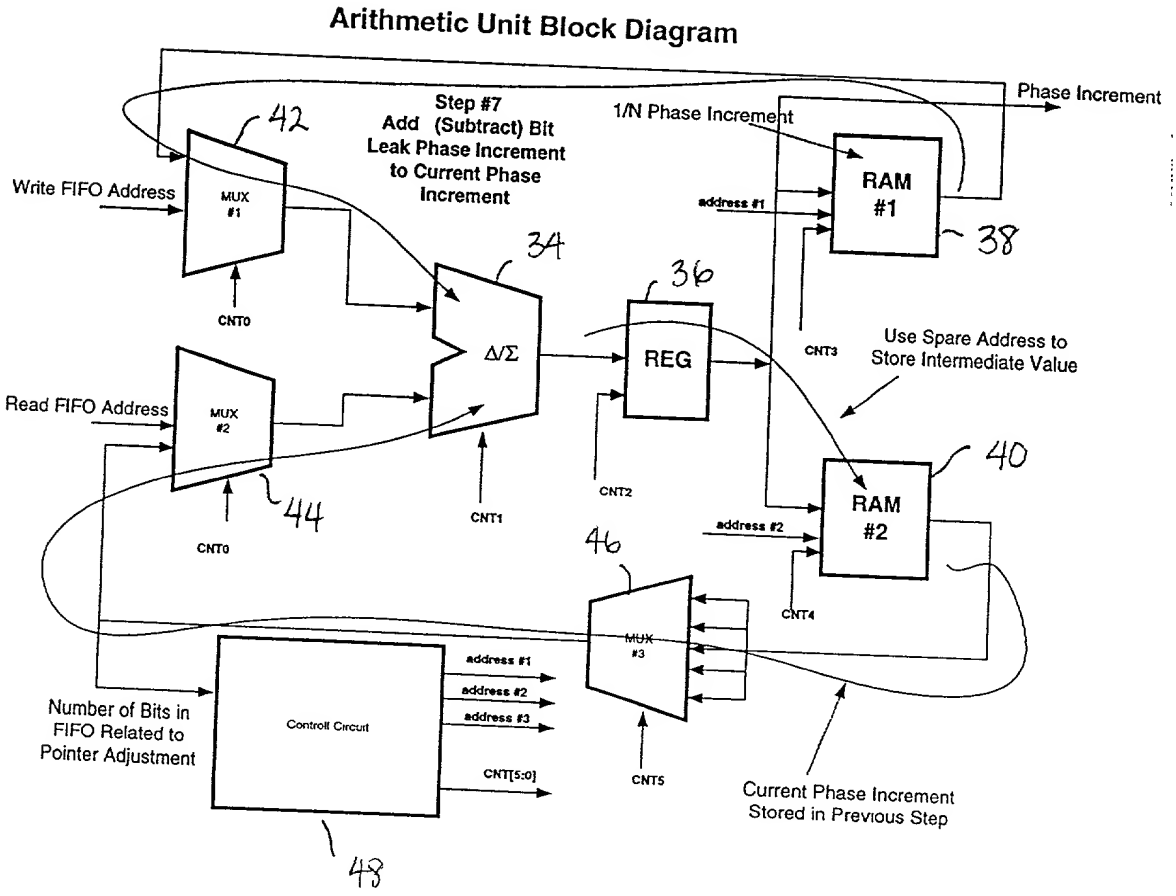
Arithmetic Unit Block Diagram
Step #7
Add (Subtract) Bit
Leak Phase Increment
to Current Phase
Increment
Phase Increment
1/N Phase Increment
Write FIFO Address
MUX
#1
42
CNT0
34
Δ/Σ
36
REG
RAM
#1
38
address #1
CNT3
Use Spare Address to
Store Intermediate Value
Read FIFO Address
MUX
#2
CNT0
44
CNT1
CNT2
40
RAM
#2
address #2
46
CNT4
MUX
#3
address #1
address #2
address #3
CNT[5:0]
Controll Circuit
Number of Bits in
FIFO Related to
Pointer Adjustment
CNT5
Current Phase Increment
Stored in Previous Step
48

Fig. 10

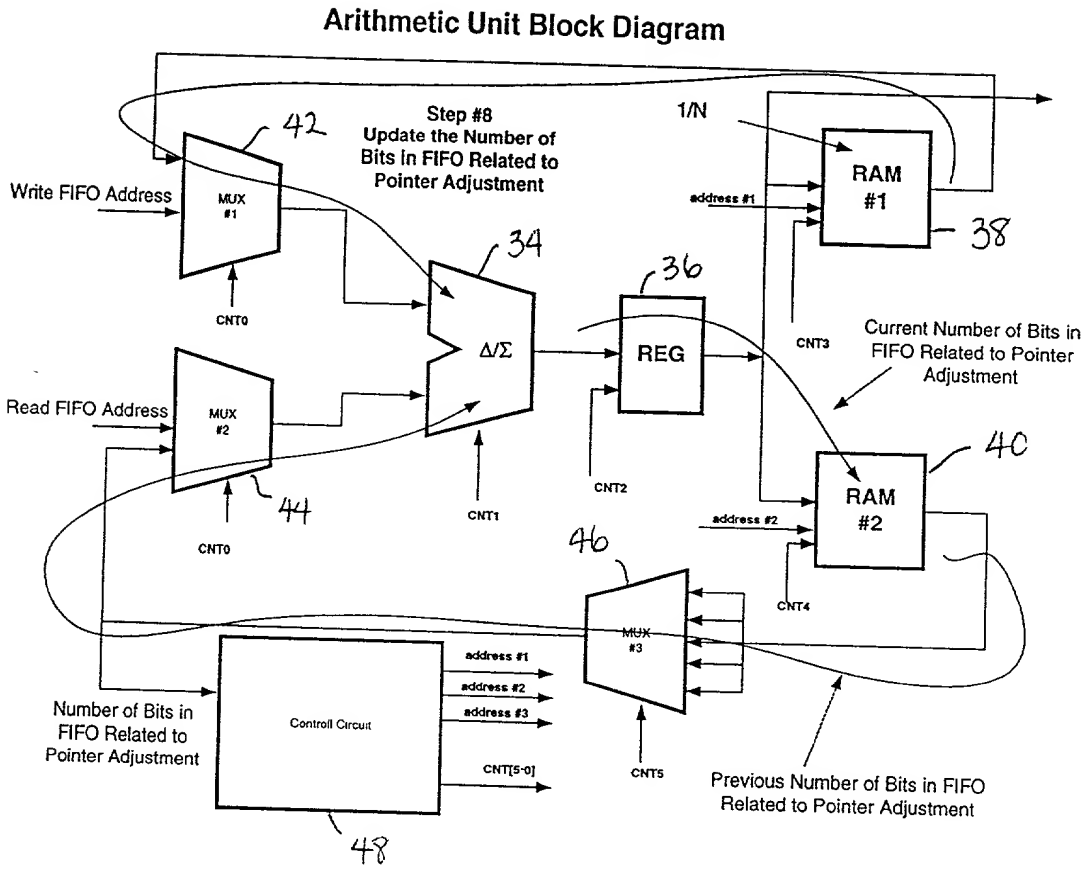
Arithmetic Unit Block Diagram
Step #8
Update the Number of
Bits In FIFO Related to
Pointer Adjustment
42
Write FIFO Address
MUX
#1
CNT0
34
Δ/Σ
36
REG
1/N
RAM
#1
38
address #1
CNT3
Current Number of Bits in
FIFO Related to Pointer
Adjustment
Read FIFO Address
MUX
#2
CNT0
44
CNT1
CNT2
40
RAM
#2
address #2
CNT4
46
MUX
#3
address #1
address #2
address #3
CNT[5-0]
CNT5
Number of Bits in
FIFO Related to
Pointer Adjustment
Controll Circuit
48
Previous Number of Bits in FIFO
Related to Pointer Adjustment

Fig. 11

Endless Phase Modulators Common Control Block

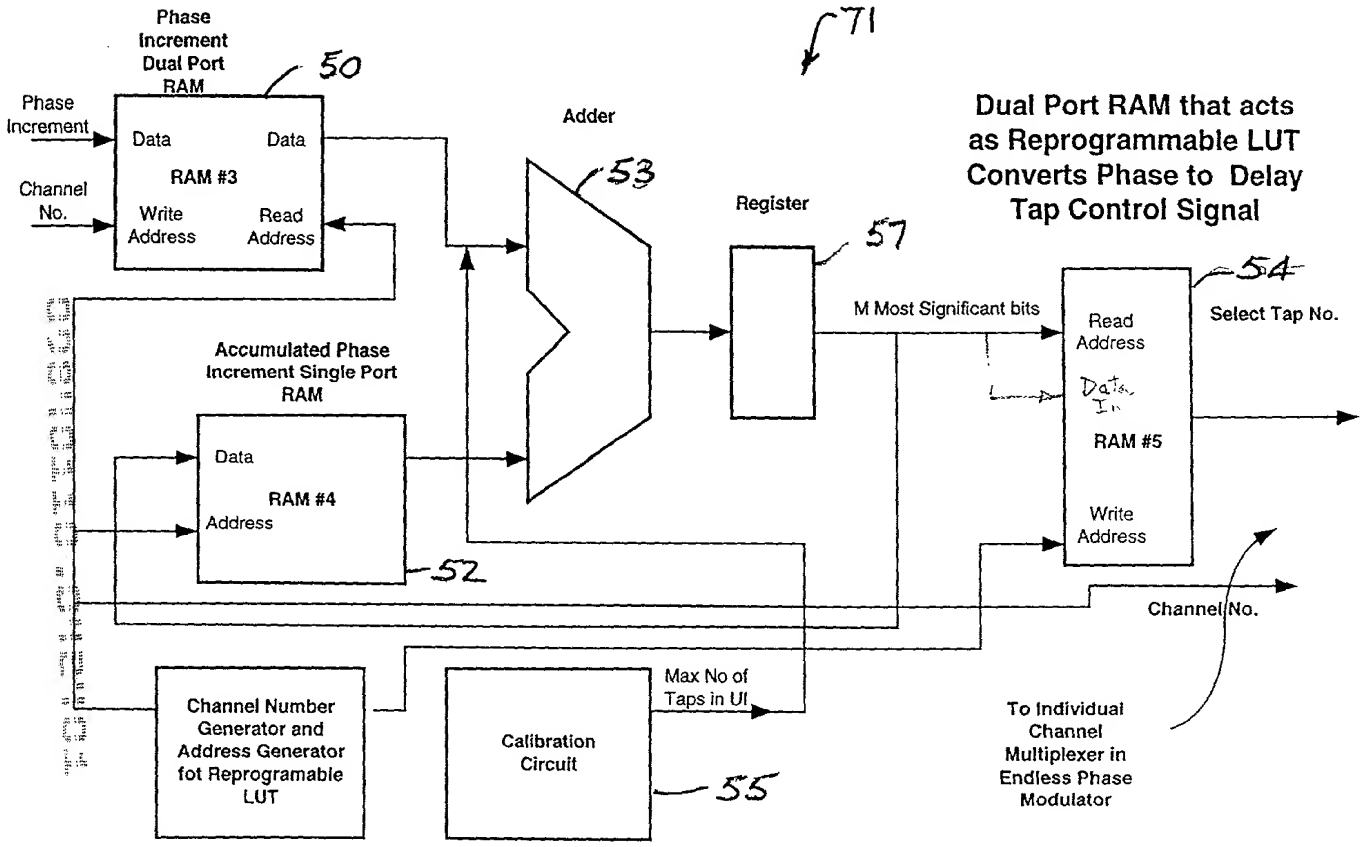

Fig. 12

Figure 13 Endless Phase Modulator Delay Line

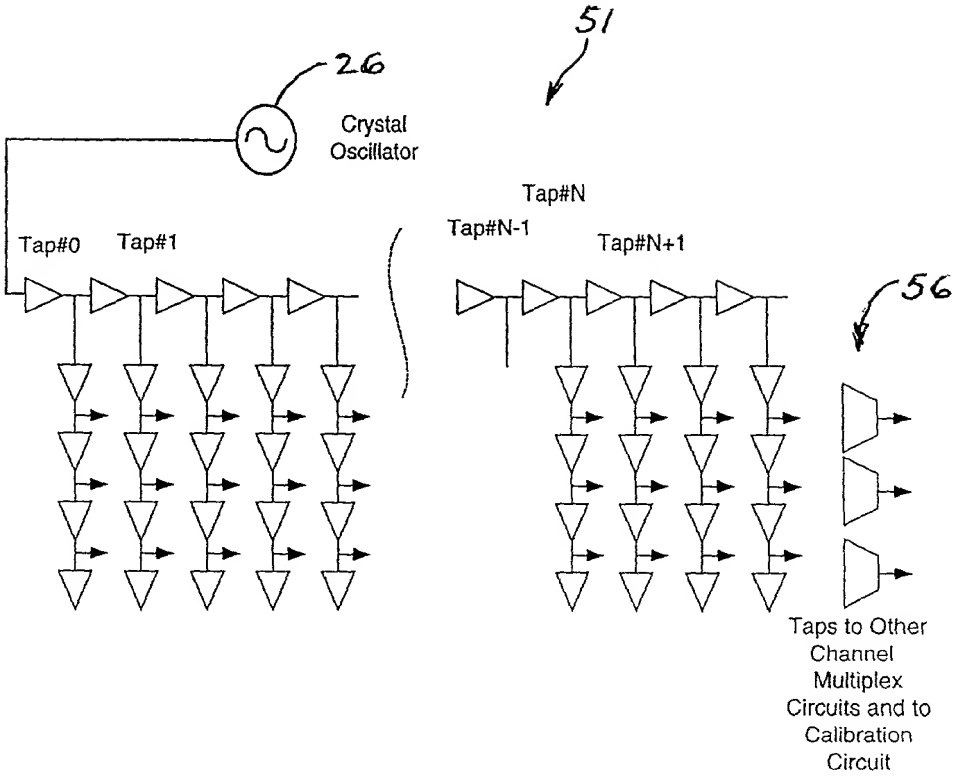

Fig. 13

Figure 14 Delay Line Calibration Circuit

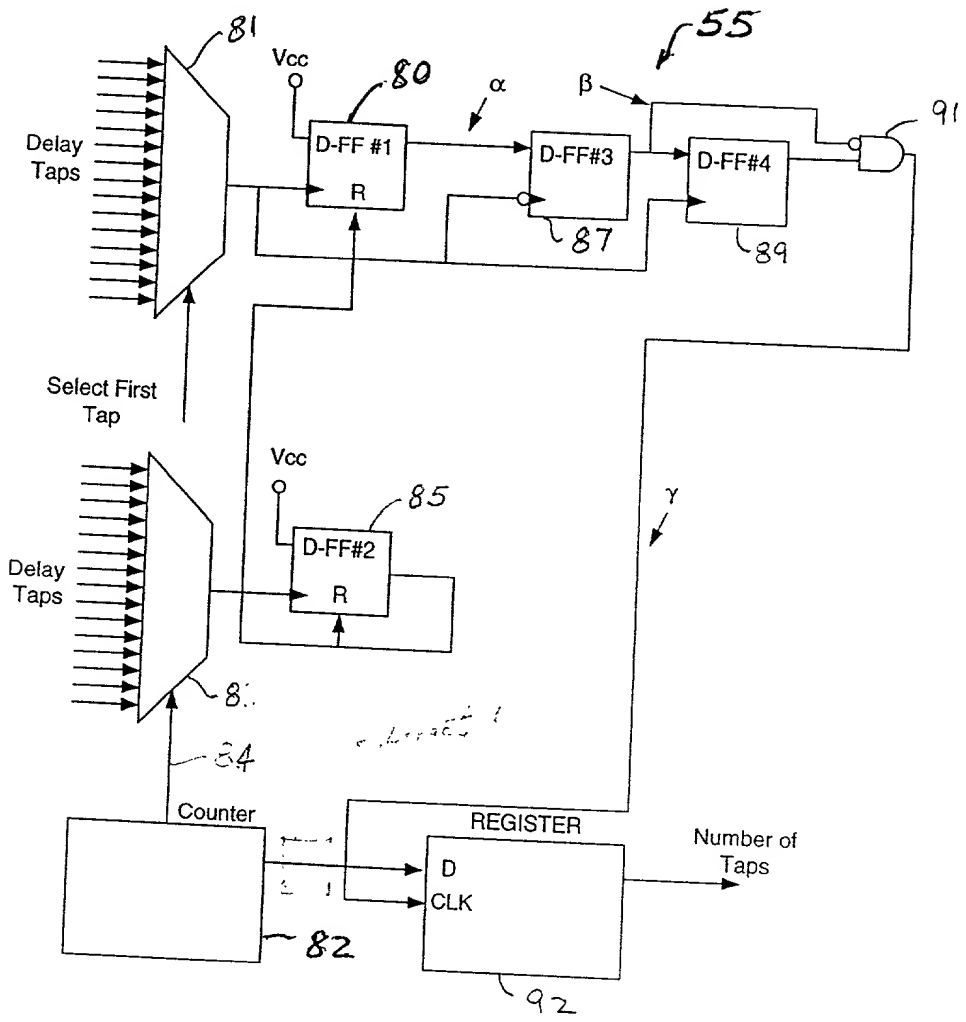

Fig. 14

Figure 15 Alternate Embodiment Using SSB Modulators

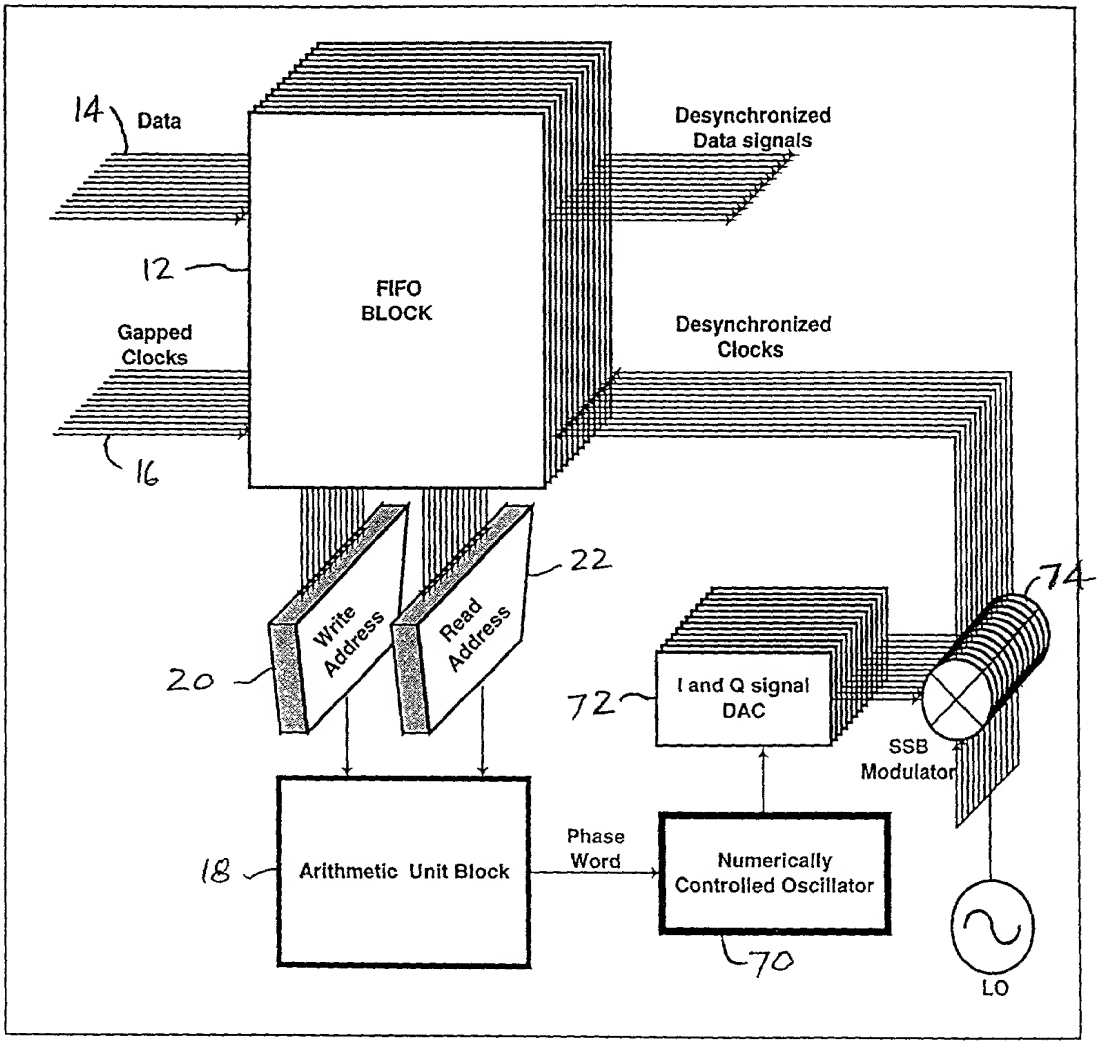

Fig. 15

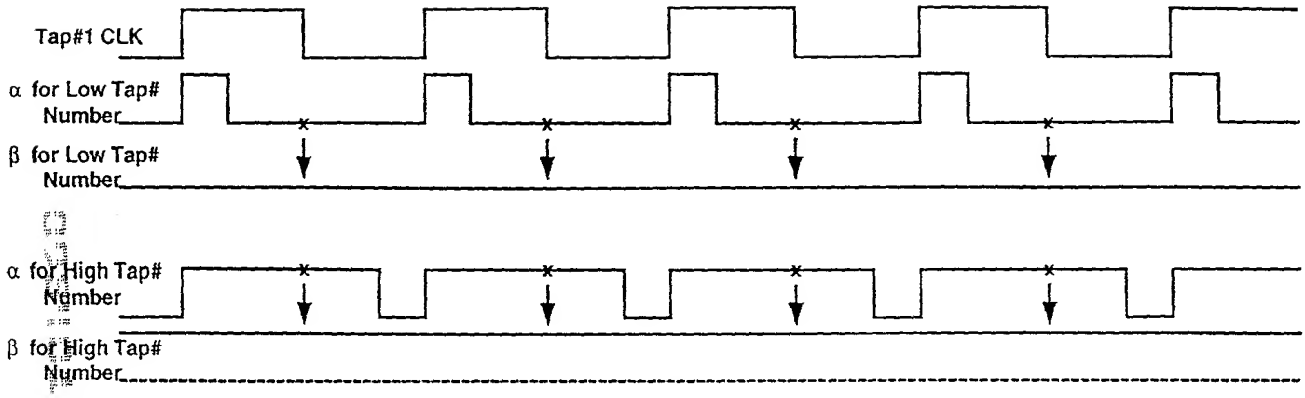
Tap#1 CLK
α for Low Tap# Number
β for Low Tap# Number
α for High Tap# Number
β for High Tap# Number

FIG 16

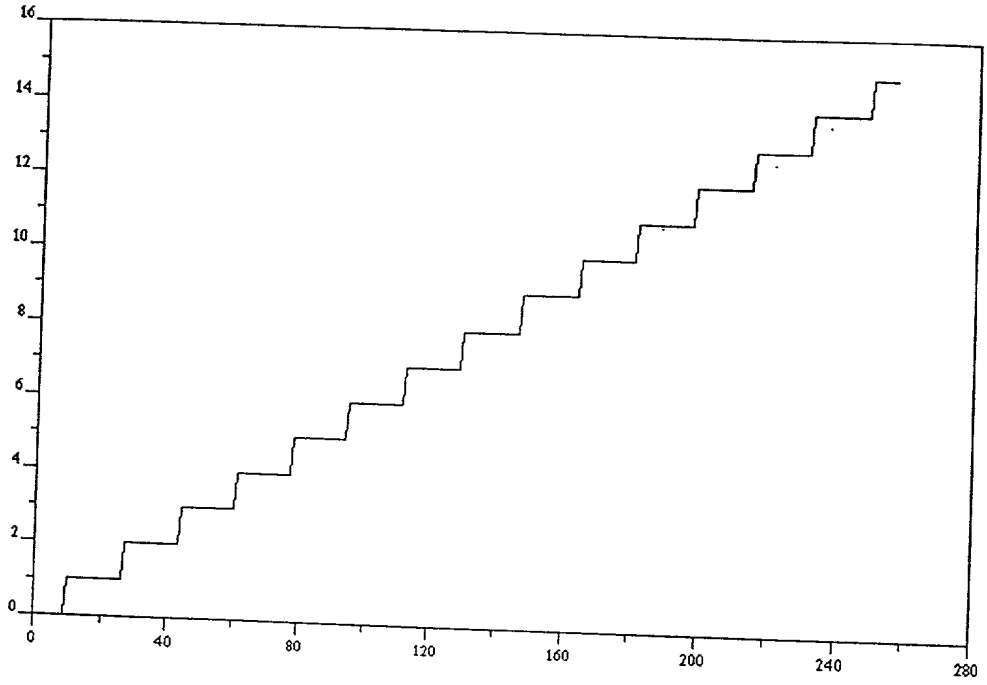
16
14
12
10
8
6
4
2
0
0
40
80
120
160
200
240
280

Fig 17

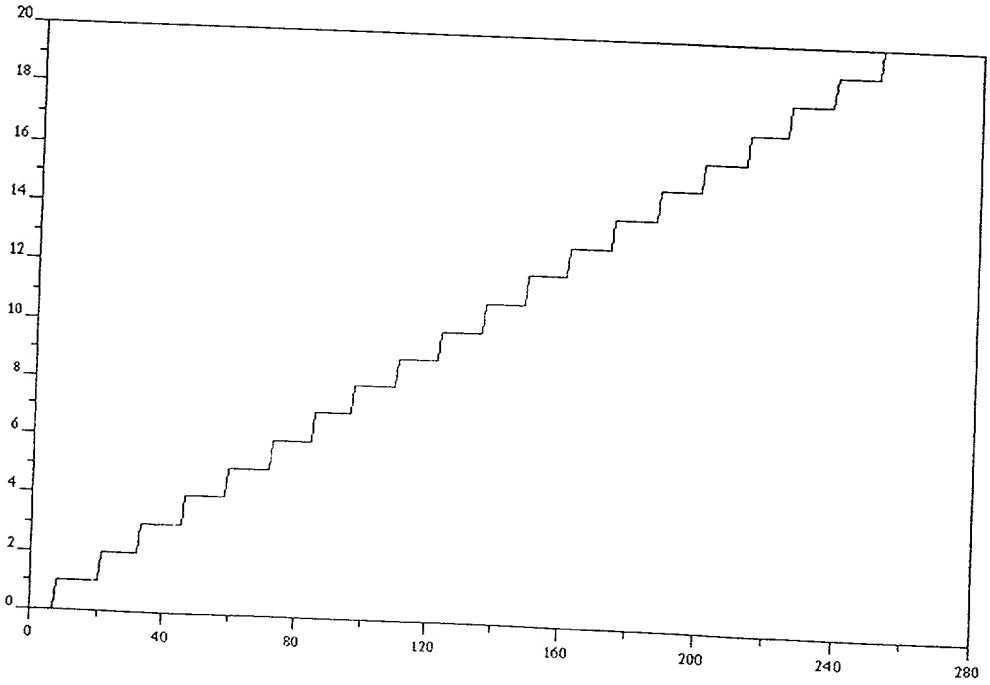
20
18
16
14
12
10
8
6
4
2
0
0
40
80
120
160
200
240
280

Fig 18